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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,156	07/06/2001	Nagahisa Watanabe	210854US2S	2834

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EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/899,156	WATANABE, NAGAHISA	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 7-16* is/are pending in the application.

4a) Of the above claim(s) *7-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *0503* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Specie election was made earlier, but during recent review it was noticed that figure number was not mentioned in the election.

Specie VI, reading on figure 31-35 elected.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 2, 3, 5, 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, "an insulting layer having first surface and a second surface located on an opposite side of said first surface and further having circuit pattern inside the insulating is layer" is not clear.

Examiner considered the insulating layer formed of multiple insulating layers with internal circuit pattern, in line with the elected specie.

Regarding claim 2, the applicant is claiming "said first plating layer is a ground work on which said second plating layer is formed, and gives conductivity to the inner surface said via". Claim 2 is depending upon claim 1, and the first plating layer is

already claimed in claim 1 and is not clear what additional structural limitation is claimed in claim 2.

Regarding claim 3, it is not clear, whether the said only one layer has flexibility or the circuit board has the flexibility. The examiner considered the board as a whole has the flexibility.

Regarding claim 5, which depend upon claim 1, the circuit pattern formed, inside the insulating layer, exposed inside the via and covered by the first plating is already claimed in claim 1. It is not clear what additional structural limitation is claimed in claim 5.

Regarding claim 14, it is not clear what is claimed by "flange portion having a shape that ***projects*** over the circuit pattern. The examiner considered a pad around the via hole.

Regarding claim 15, the applicant is claiming the second plating layer has a flange portion laminated of said flange portion of said first plating layer. The word "laminated" is not clear. If the "laminated" is the second plating layer, than the second plating layer is already claimed in claim 1 and claim 15 is indirectly depending upon claim 1.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 5 and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by L. J. Quintana, US Patent No. 3,471,631.

Regarding claim 1,2 and 5 Quintana discloses a printed wiring board, comprising:

an insulating layer having a first surface, and a second surface located on an opposite side of said first surface (see figure 7, top surface and a bottom surface),

a plurality of circuit patterns formed by etching metal foils laminated on at least said first surface and said second surface of said insulating layer, wherein a circuit pattern on the first surface of said plurality of circuit patterns is a line through which an electric current flows (circuit patterns on top and bottom layer, see figure 7);

a via formed on said insulating layer, said via having one end opened on said first surface of said insulating layer and the other end closed by a circuit pattern of said plurality of circuit patterns formed on a part of said insulating layer other than said first surface (via 16, see figure 2);

a first plating layer having a first portion that covers an inner surface of said via

and a circuit pattern of said plurality of said circuit patterns that closes said other end of said via and which is exposed within said via, a second portion that covers a circuit pattern of said plurality of said circuit patterns that is on said first surface and which continues to said one end of said via, and a third portion that covers a part of said circuit pattern of said plurality of circuit patterns formed on the first surface at a location outside the via, wherein, the first to third portions are simultaneously processed (electroless layer 20, see figure 3, column 2, line 65-68); and

a second plating layer laminated on said first plating layer and electrically connecting said circuit pattern of said plurality of circuit patterns formed on said first surface with said circuit pattern of the plurality of circuit patterns that closes said other end of said via, wherein, the second plating layer and the third portion of the first plating layer form a thick portion having an increased thickness on a part of said circuit pattern formed on the first surface, and a current capacity of the circuit pattern is increased at the thick portion (electroplating layer 22, see figure 4, though electroless plating layer is not shown in figure 4, it is inherently there. As the electroless layer is preferably used as groundwork for making the non-conductive dielectric layer inside the via ready to be receptive to the subsequent electroplating of the required thickness).

Regarding claims 14 and 15, Quintana further discloses a flange portion, see figure 7, area around the via opening.

Regarding claim 16, Quintana further discloses circuit pattern with thick portion, see figure 7, portion extended beyond via hole towards left on top surface.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over L. J. Quintana, US Patent No. 3,471,631, as applied to claim 1-2, 5 and 14-16, in view of Foster et al., US Patent No. 5,108,553, hereafter, Foster.

Regarding claim 3, the applicant is claiming the flexibility of the insulating layer. Though, Quintana does not disclose about flexibility or rigidity of the board, the flexibility will depend upon the type of material used for insulating layer. The use of flexible insulating substrate is known in the art for the apparent reason of having flexibility during installation and the operation.

Foster discloses one such flexible circuit board with blind via.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Quintana with flexibility, as taught by Foster, apparently, in order to have the flexibility during installation and the operation.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, 5 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Shin et al., US Patent No. 6,405,431, hereafter Shin.

Regarding claim 1,2 and 5 Shin discloses a printed wiring board, comprising:

an insulating layer having a first surface, and a second surface located on an opposite side of said first surface (see figure 4g and 6c, top surface and a bottom surface),

a plurality of circuit patterns formed by etching metal foils laminated on at least said first surface and said second surface of said insulating layer, wherein a circuit pattern on the first surface of said plurality of circuit patterns is a line through which an electric current flows (circuit patterns on top and bottom layer, see figure 4g and 6c);

a via formed on said insulating layer, said via having one end opened on said first surface of said insulating layer and the other end closed by a circuit pattern of said plurality of circuit patterns formed on a part of said insulating layer other than said first surface (via on top surface, see figure 4g and 6c);

a first plating layer having a first portion that covers an inner surface of said via and a circuit pattern of said plurality of said circuit patterns that closes said other end of said via and which is exposed within said via, a second portion that covers a circuit pattern of said plurality of said circuit patterns that is on said first surface and which continues to said one end of said via, and a third portion that covers a part of said circuit pattern of said plurality of circuit patterns formed on the first surface at a location outside the via, wherein, the first to third portions are simultaneously processed (an electroless and electro copper plating carried out on board, see column 7, line 64-67); and

a second plating layer laminated on said first plating layer and electrically connecting said circuit pattern of said plurality of circuit patterns formed on said first surface with said circuit pattern of the plurality of circuit patterns that closes said other end of said via, wherein, the second plating layer and the third portion of the first plating layer form a thick portion having an increased thickness on a part of said circuit pattern formed on the first surface, and a current capacity of the circuit pattern is increased at

the thick portion (an electroless and electro copper plating carried out on board, see column 7, line 64-67).

Regarding claims 14 and 15, Quintana further discloses a flange portion, see figure 4g and 6c, area around the via opening.

Regarding claim 16, Quintana further discloses circuit pattern with thick portion, see figure 4f and 6c.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al., US Patent No. 6,405,431, hereafter Shin, as applied to claims 1-2,5 and 14-16, in view of Foster et al., US Patent No. 5,108,553, hereafter, Foster.

Regarding claim 3, the applicant is claiming the flexibility of the insulating layer. Though, Quintana does not disclose about flexibility or rigidity of the board, the flexibility will depend upon the type of material used for insulating layer. The use of flexible

insulating substrate is known in the art for the apparent reason of having flexibility during installation and the operation.

Foster discloses one flexible circuit board with blind via.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Quintana with flexibility, as taught by Shin, apparently, in order to have the flexibility during installation and the operation.

Response to Arguments

12. Applicant's arguments with respect to claims 1-3, 5 and 14-16 have been considered but are moot in view of the new ground(s) of rejection. Further,

Burgess, US Patent No. 4,642,160, as applied earlier, discloses the blind via with plating inside the via and the circuit pattern, with electroless plating only. However, it is known and preferred in the art to have a thin electroless layer followed by primary electroplating to the desired thickness, see, Printed Circuit Handbook by Clyde F. Coombs, J., Fourth Edition, page 3.11, paragraph 3.8.2. Therefore, it would have been obvious to one having ordinary skill in the art at time the invention was made to provide the circuit board of Burgess with first and second plating layer to have better electrical conductivity through the via with the required thickness.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Haruta et al., discloses a multilayer circuit board with blind hole and disclose in the background disclosure, the panel subjected to conventional electroless copper plating and electrolytic copper plating to form plated through hole, see column 1, line 34-40.

Chakravorty et al., discloses electronic circuits board with a seed layer such as electroless copper, followed by electrolytic plating layer on seed layer, column 4, line 1-5.

Masuo et al., and Yoshihiko discloses multilayer circuit board with electroless copper followed by the electrolytic copper.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (8:30 - 5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp
May 31, 2003

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